IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Chambers et al.	Art Unit:	2818
Serial No.:	10/696,539	Examiner:	Tran, M.
Filing Date:	10/29/2003	Docket No.:	TI-36031
Customer No.:	23494	Conf. No.:	7816

Title: TRIPLE-GATE MOSFET TRANSISTOR AND METHODS FOR FABRICATING THE SAME

ELECTION

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as first Class Mail in an envelope addressed to Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

10-7-04
Date
Marianna Smith
Marianna Smith

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

With respect to the Restriction Requirement mailed on 09/27/2004, the Examiner has restricted the instant application to the invention of Group I (Claims 11-24), or Group II (Claims 1-10). In light of this, Applicants elect to pursue Group II, (Claims 1-10) without traverse.

Respectfully submitted,

Jacqueline J. Garner
Attorney for Applicant
Reg. No. 36,144

Texas Instruments Incorporated
P.O. Box 655474, M/S 3999
Dallas, TX 75265
(214) 532-9348 or
(972) 917-5643
Fax: (972) 917-4418